

REMARKS

Summary of Claim Status

Claims 1-23 are pending in the present application. Claims 1, 5-17, 19, and 21-23 are rejected for the reasons discussed below.

Claims 2-4, 18, and 20 are objected to as depending from a rejected base claim, but would be allowable if properly rewritten in independent form.

Applicant requests the favorable reconsideration of the claims and withdrawal of the pending rejections and objections, in view of the present amendment and in light of the following remarks.

Rejections Under 35 USC 102(e)

Claims 1, 5-17, 19, and 21-23 are rejected as being anticipated by Kunikiyo (U.S. Patent No. 6,538,954 B2, hereinafter Kunikiyo). The Examiner therefore argues that Kunikiyo teaches every element of every claim, either expressly or by implication. (MPEP 706.02, pg. 700-20, provides the following summary of the relevant standard: "For anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present.") Applicant respectfully disagrees.

Claims 19 and 21-23

The Office Action states:

Regarding to [*sic*, regarding] claims 19, 21-23, Kunikiyo discloses a memory cell for suppressing sub-threshold leakage in a transistor, the memory comprising: a plurality of transistors (MC, RK) configur[able] to store a value, wherein the value can under-drive the transistor in its off state, wherein if the transistor if [*sic*, is] a PMOS device having a source/gate voltage of VDD and the memory cell drives a gate/source of the transistor, the value is slightly more positive/slightly less than VDD ($V_{dd} + V_{thn}/V_{dd} - 2V_{thn}$), and wherein if the transistor is a NMOS device having a gate voltage of VSS and the memory cell drives a source of the transistor, then the value is slightly more positive than VSS. *See Figs. 2-10, 13-27; Cols. 12-23.*

Applicant is confused by this characterization of the reference. Kunikiyo does not teach or suggest a memory cell storing a value that can under-drive a transistor in its off state. Therefore, the relevance of Kunikiyo to the present claimed invention is very unclear. Further, the portions of the reference cited in the rejection are so broad as to fail to assist in the attempt to identify such a memory cell.

Applicant respectfully draws the Examiner's attention to 37 CFR 1.104(c)(2), which states:

When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

The pertinence of the reference should be explained because none of the cited figures or text of Kunikiyo illustrate or describe a memory cell storing a value that can under-drive a transistor in its off state.

Because the Kunikiyo reference appears to be irrelevant to the claimed invention, Claims 19 and 21-23 are allowable over the cited reference.

Claims 1 and 5-17

Regarding Claims 1 and 5-17, the Office Action simply includes a broad, conclusory statement:

With regard to claims 1 and 5-17, they encompass the same scope of invention as to that of claims 19, 21-23 except they draft [*sic*, are drafted] in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

This statement completely ignores many limitations present in the claims. For example, none of Claims 19, 21-23 includes a set of limitations that exactly corresponds to those of Claim 1. Claim 1 includes limitations directed to "storing a value in a memory cell coupled to a gate of the transistor" and "applying a gate to source voltage to the transistor that under-drives the transistor", neither of which are included in Claims 19, 21-23. Claim 19 specifies that the circuit "can under-drive the

transistor in its off state." Claims 21-23 include specific limitations regarding NMOS and PMOS devices. None of these limitations are included in Claim 1. This is just one of many examples illustrating that it is inappropriate to apply a broad rejection to all of the method claims based on the rejection of structural Claims 19, 21-23.

Applicant respectfully requests that, if the rejection is maintained, the next Office Action include specific recitations of portions of the cited reference that anticipate the limitations of each of Claims 1 and 5-17.

Request for Non-Final Action

If an action other than allowance of the pending claims is to be made, Applicant respectfully requests that the next action be a non-final action.

37 CFR 1.104(c)(2) states that:

When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

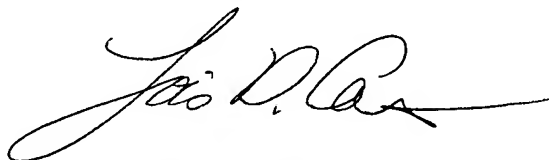
The pertinence of the cited reference should be clearly explained, because it is not clear where the reference shows the cited claim elements, if they are indeed taught or suggested in any way.

Further, MPEP 707.07(d) states that "a plurality of claims should never be grouped together in a common rejection, unless that rejection is equally applicable to all claims in the group." As apparatus and method claims have been grouped together without explanation, Applicant hereby requests a new non-final action if the pending claims are not allowed.

Conclusion

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested. If any action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicant's agent, Lois D. Cartier, at 720-652-3733.

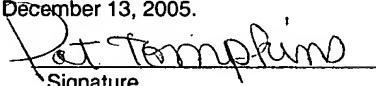
Respectfully submitted,



Lois D. Cartier
Agent for Applicant
Reg. No. 40,941

I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on December 13, 2005.

Pat. Tompkins
Name


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